SID1152K circuit layout suggestion
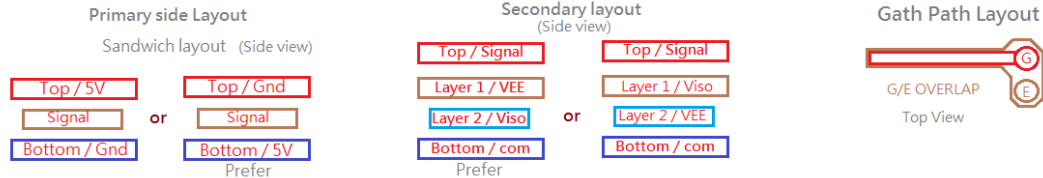
2017/09/25 Romeo

IGBT (No Short circuit protection)

SCALE-iDriver

Reduce impedance/ increase noise rejection
5V PWM: R1/R2=20/475 ohm
15V PWM: R1/R2=1.15k/348 ohm
(0805 size)

Primary-Side Logic

Secondary-Side Logic

Command Signal

R_1

IN

SO

VCC

VCC

GND

C_F 100pF

R_2

C_1 4.7 µF

GND

FluxLink

VCE

1 kΩ

VGXX

C_{GXX} 10 nF

VISO

4.7 µF

GH

V_{TOT}

GL

D_{STO}

R_{GON}

Gate

R_{GOFF}

R_{GE}

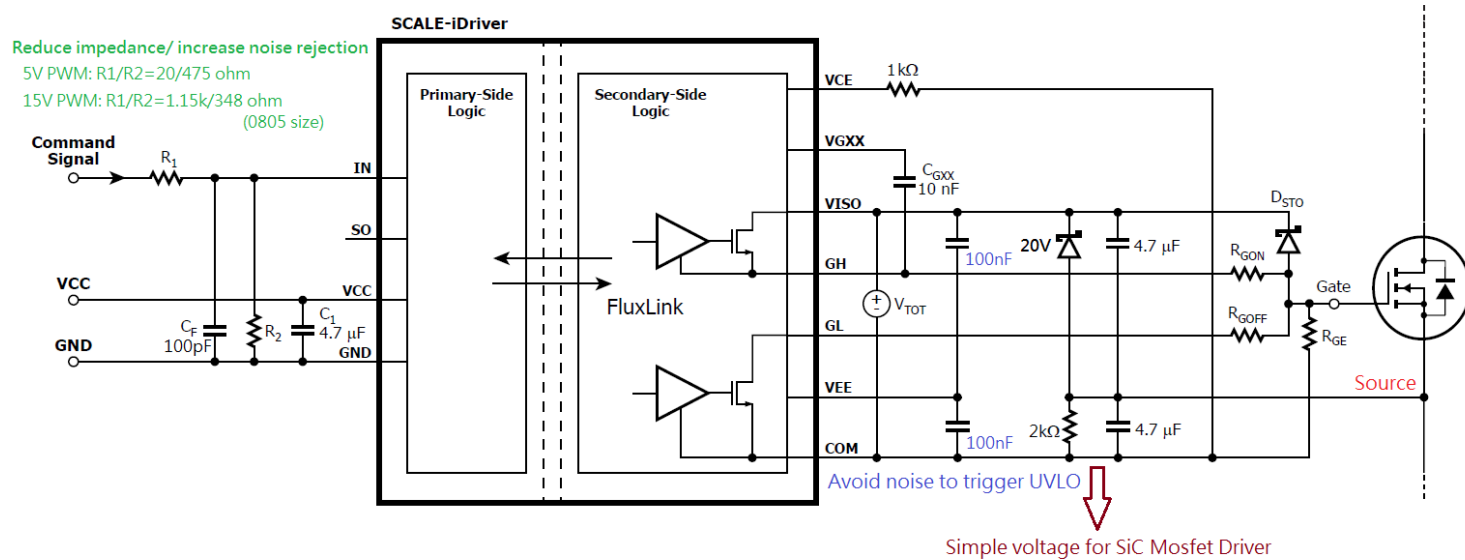Collector

Emitter

4.7 µF

COM

2018/07/09
2018/07/09
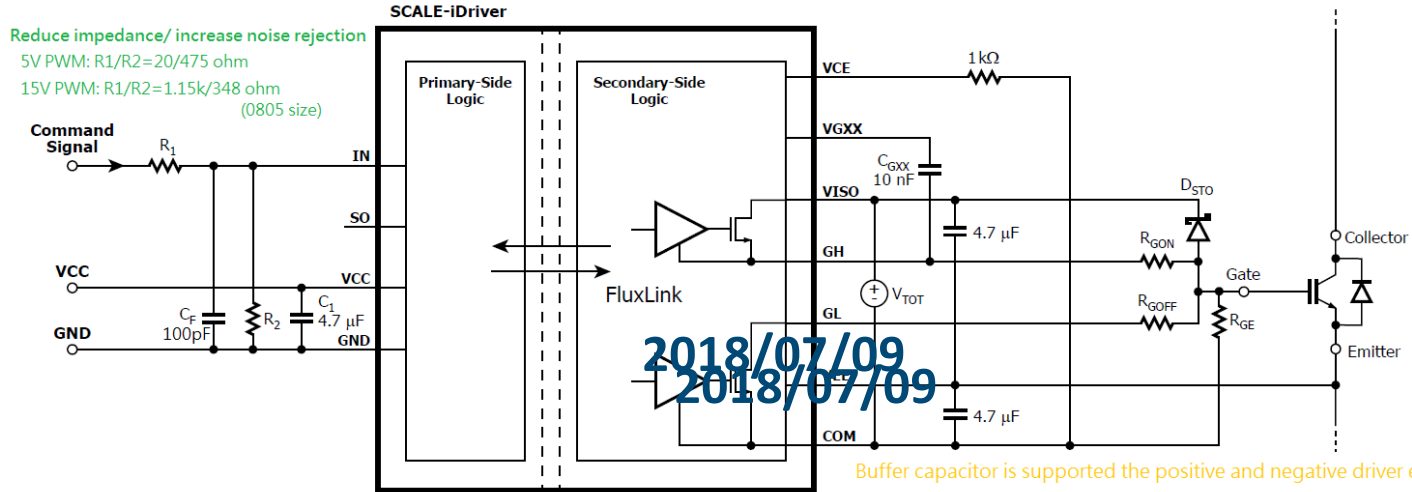
Buffer capacitor is supported the positive and negative driver energy.
It is needed to as close each pin as possible.
Use 50V capacitor instead of 25V version

COMMON layout suggestion

Primary side Layout
Sandwich layout (Side view)

Top / 5V	
Signal	or
Bottom / Gnd	

Prefer

Top / Gnd
Signal
Bottom / 5V

Secondary layout
(Side view)

Top / Signal	
Layer 1 / VEE	or
Layer 2 / Viso	
Bottom / com	

Prefer

Top / Signal
Layer 1 / Viso
Layer 2 / VEE
Bottom / com

Gath Path Layout

G/E OVERLAP
Top View

G
E

SiC Mosfet (No Short circuit protection)

SCALE-iDriver

Reduce impedance/ increase noise rejection
5V PWM: R1/R2=20/475 ohm
15V PWM: R1/R2=1.15k/348 ohm
(0805 size)

Command Signal

R_1

Primary-Side Logic

Secondary-Side Logic

IN

SO

VCC

GND

VCC

C_F 100pF

R_2

C_1 4.7 µF

FluxLink

VCE

1 kΩ

VGXX

C_{GXX} 10 nF

VISO

D_{STO}

GH

100nF

20V

4.7 µF

R_{GON}

Gate

GL

V_{TOT}

R_{GOFF}

R_{GE}

VEE

Source

COM

100nF

2kΩ

4.7 µF

Avoid noise to trigger UVLO

Simple voltage for SiC Mosfet Driver

COMMON layout suggestion

Primary side Layout
Sandwich layout (Side view)

Top / 5V		Top / Gnd
Signal	or	Signal
Bottom / Gnd		Bottom / 5V

Prefer

Secondary layout
(Side view)

Top / Signal		Top / Signal
Layer 1 / Source	or	Layer 1 / Viso
Layer 2 / Viso		Layer 2 / Source
Bottom / com		Bottom / com

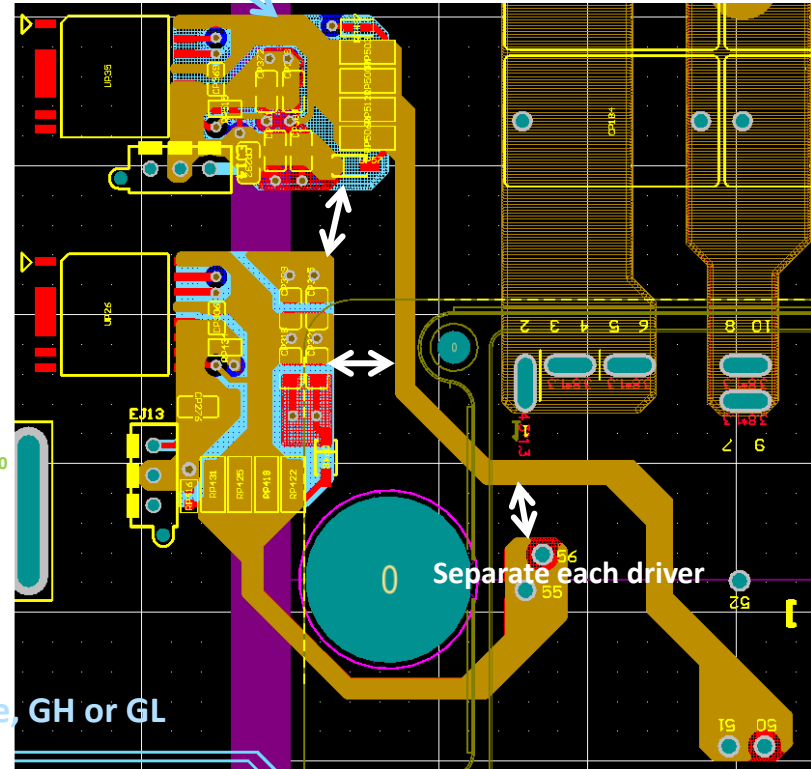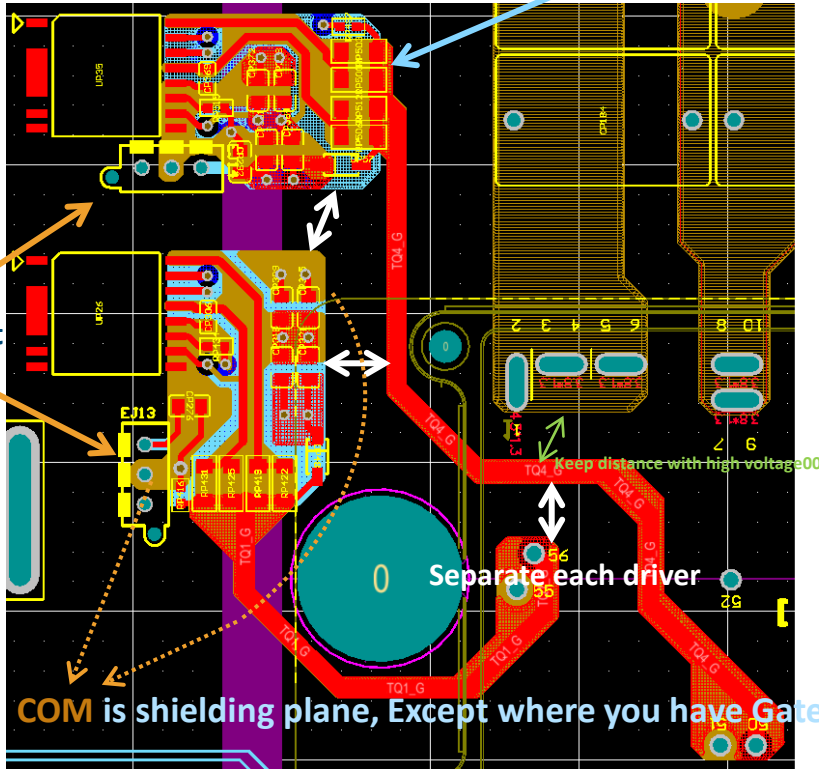Prefer

Gath Path Layout

G/S OVERLAP
Top View

Remark:

- **Schottky diode (D_{STO}) connected between semiconductor gate and VISO pin. The short-circuit current value can be limited to a safe value.**

- **Since the desaturation detect function is disable, the diode can be omitted to gain more layout size.**

- **Disable desaturation function**

  ▷ V_{CE} is a input pin.

  ▷ Input pins of an IC are often connected to the gate of a MOS transistor or input of a OPAMP. This input often has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, V_{CE} pin should be connected one 1k ohm resistor to the power supply or ground line.

Explain Design1

One Channel Layout Explain

TOP Layer (Connect all component)

Mid Layer2 (Viso Plane)

Mid Layer1 (VEE Plane)

Bottom Layer (COM Plane)

Remark: Gate and VEE are always together

VEE / Viso / COM Planes are important to improve "EMC behavior"

Explain2: Top/Mid-Layer1

Gate & VEE always together(VEE only cross gate loop)

Separate Aux connect

Separate each driver

Separate each driver

Keep distance with high voltage00

COM is shielding plane, Except where you have Gate, GH or GL

Explain2: Mid-Layer2/Bottom

Viso / COM shielding plane